System Overview

This high-performance, high-voltage power supply is optimized to charge a dedicated **Main Pulse Storage Bank** for a **100 kW peak** pulsed system operating at a **20 kV DC target voltage**. It utilizes a single-phase, high-frequency LLC resonant converter driving a modular 4-transformer matrix to overcome the insulation, parasitic capacitance, and thermal limits of high-voltage engineering.

🔧 **Key Component Breakdown**

1. Primary Power Stage

- **Topology:** Single high-power **Full-Bridge Inverter** utilizing Silicon Carbide (SiC) MOSFET dual-modules ("bricks").
- **Resonant Tank:** A single high-current resonant capacitor bank (C_{r}) and series resonant inductor (L_{r}).
- **Operation:** Operates with Zero Voltage Switching (ZVS) on the primary side, switching between 50 kHz and 150 kHz to optimize efficiency and minimize magnetic sizes.

2. The 4-Transformer Matrix

- **Configuration:** Four identical high-voltage step-up transformers arranged in a physically symmetrical 2×2 grid layout to equalize wire lengths and balance leakage inductances.
- **Primary Side:** All four primary windings are **wired in series** into a single loop fed by the resonant tank. This naturally forces an identical primary current through every transformer, ensuring perfect energy and voltage distribution.
- **Secondary Side:** Each transformer features an independent secondary winding designed to isolate and output exactly **5 kV AC**. Splitting 20 kV into four 5 kV steps drastically reduces the destructive parasitic winding capacitance (C_{s}) and simplifies the physical insulation barriers.
- **Insulation:** The complete 4-transformer matrix is vacuum-encapsulated in high-purity dielectric epoxy or silicone to prevent air gaps, corona discharge, and internal arcing.

3. Stacked Output Rectification & Filtering

- **Rectifiers:** Four independent full-wave bridge rectifiers—one mounted directly to the secondary of each transformer. Built using **10 kV-rated Silicon Carbide (SiC) Schottky diodes**, giving an excellent 2:1 voltage safety margin with zero reverse-recovery noise.
- **Distributed Capacitors (Filters Only):** Four separate **5 kV DC polypropylene film capacitors** (small values, e.g., 1 nF to 10 nF) are connected directly across the DC output of each respective rectifier stage. They provide a tiny high-frequency AC loop path to clamp 100 kHz switching noise at the source and act as dynamic voltage dividers. They do **not** provide power to the pulse.

- **Series Combination:** The DC outputs of the four 5 kV rectifier-capacitor blocks are wired together in a single **series chain** to cleanly sum up to a unified **20 kV DC charger output**.

4. The Main Pulse Storage Bank (The Actual Load)

- **The Component:** A single, large, heavy-duty **20 kV DC pulse-discharge capacitor** (typically 100 nF to several microfarads) sits at the final output of the system.
- **The Function:** This capacitor is the **actual energy source** that dumps the 100 kW pulse into the radar switch. Because the LLC charger is too slow to provide 100 kW instantaneously on a microsecond scale, this reservoir stores energy slowly over milliseconds and dumps it in microseconds.
- **The Isolation:** A high-voltage **blocking diode string** or a **charging choke (inductor)** is placed between the 4 stacked rectifier stages and this Main Pulse Capacitor. This isolation prevents the violent 100 kW pulse discharge from snapping backward into the 5 kV filter capacitors, protecting the rectifiers from instant overvoltage destruction.

🎛️ Control Loop Strategy

The system utilizes a **Cascaded (Two-Tier) Digital Control Loop** implemented via a high-performance DSP or FPGA. It combines a single outer voltage loop with internal current-averaging mechanisms:

- **Outer Master Voltage Loop:** A high-voltage resistor divider monitors the final **20 kV Main Pulse Capacitor**.
    - Because a discharged pulse capacitor looks like a dead short circuit, this outer loop commands a very high base switching frequency (f_{sw}) well above resonance right after a pulse fires.
    - As the main capacitor charges, the outer loop smoothly sweeps the base frequency down toward resonance to increase converter gain and maintain a steady constant-current charging profile.
- **Inner Average Current Loops:** To prevent high-frequency noise from your 100 kW pulse from corrupting the controls, the system relies on **Average Current Mode Control (ACMC)** rather than peak current sensing.
    - Current transformers (CTs) on the primary side continuously measure the high-frequency resonant current waveforms.
    - The digital controller integrates these signals on a cycle-by-cycle basis to compute the true average current passing through the primary chain.
    - If component manufacturing tolerances create a slight power imbalance, these inner loops introduce microscopic, symmetrical adjustments to the **Asymmetric PWM Duty Cycle** or **Phase-Shift Trimming ($\Delta\theta$)** of the primary switches. This forces

the 100 kW load to distribute perfectly across the primary switches and ensures exactly 5 kV DC is maintained across all four output stages.

- **Target Stop:** Once the outer voltage loop registers that the main 20 kV reservoir is completely full, the controller enters a rapid burst/skip mode to freeze energy transfer instantly, preventing voltage overshoot before the next 100 kW discharge pulse hits.
